

## XCVR-V10U02-I-AO

Ciena® XCVR-V10U02 Compatible TAA Compliant 25GBase-BX SFP28 Transceiver (SMF, 1330nmTx/1270nmRx, 10km, LC, -40 to 85C)

### Features

- SFF-8402 and SFF-8472 Compliance
- Simplex LC Connector
- Industrial Temperature -40 to 85 Celsius
- Single-mode Fiber
- Hot Pluggable
- Excellent ESD Protection
- Metal with Lower EMI
- RoHS Compliant and Lead Free



### Applications

- 25GBase Ethernet
- Access and Enterprise

### Product Description

This Ciena® SFP28 transceiver provides 25GBase-ER throughput up to 40km over single-mode fiber (SMF) using a wavelength of 1310nm via an LC connector. It is guaranteed to be 100% compatible with the equivalent Ciena® transceiver. This easy to install, hot swappable transceiver has been programmed, uniquely serialized and data-traffic and application tested to ensure that it will initialize and perform identically. Digital optical monitoring (DOM) support is also present to allow access to real-time operating parameters. This transceiver is Trade Agreements Act (TAA) compliant. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

AddOn's transceivers are RoHS compliant and lead-free.

TAA refers to the Trade Agreements Act (19 U.S.C. & 2501-2581), which is intended to foster fair and open international trade. TAA requires that the U.S. Government may acquire only "U.S. – made or designated country end products."



### Regulatory Compliance

- ESD to the Electrical PINs: compatible with MIL-STD-883E Method 3015.4
- ESD to the LC Receptacle: compatible with IEC 61000-4-3
- EMI/EMC compatible with FCC Part 15 Subpart B Rules, EN55022:2010
- Laser Eye Safety compatible with FDA 21CFR, EN60950-1& EN (IEC) 60825-1,2
- RoHS compliant with EU RoHS 2.0 directive 2015/863/EU

### Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Maximum Supply Voltage	Vcc	0		3.6	V	+3.3V
Storage Temperature	TS	-40		85	°C	
Operating Case Temperature	Tc	-40	25	85	°C	
Optical Receiver Input	Pmax			+5.5	dBm	Average

### Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Power Supply Voltage	Vcc	3.135	3.30	3.465	V	
Power Supply Noise	Vrip			2 3	% %	DC – 1MHz 1 – 10MHz
Power Consumption	Pw			1.2	W	

## High Speed Electrical Characteristics

Parameter	Test Point	Min.	Typ.	Max.	Unit	Notes/ Conditions
<b>High Speed Electrical Input Characteristics</b>						
Overload differential voltage (peak-to-peak)	TP1a	900			mV	Calibrated at TP1a Note 3: Section 13.3.12
Differential termination mismatch	TP1			10	%	At 1 MHz Note 3: Section 13.3.6
Differential return loss (SDD11)	TP1			Note 1	dB	
Common mode to differential conversion and differential to common mode conversion (SDC11, SCD11)	TP1			Note 2	dB	
<b>High Speed Electrical Output Characteristics</b>						
Differential voltage, pk-pk	TP4			900	mV	
Common mode noise, RMS	TP4			17.5	mV	Note 6: Section 13.3.5
Differential termination mismatch	TP4			10	%	At 1 MHz
Differential return loss (SDD22)	TP4			Note 4	dB	
Common mode to differential conversion and differential to common mode conversion (SDC22, SCD22)	TP4			Note 5		
Transition Time, 20 to 80%	TP4	9.5			ps	Note 6: Section 13.3.10
Vertical Eye Closure (VEC)				5.5	dB	Note 6: Section 13.3.11
Eye width at 10-15 probability (EW15)	TP4	0.57			UI	Note 6: Section 13.3.11
Eye height at 10-15 probability (EH15)	TP4	228			mV	Note 6: Section 13.3.11

### Notes:

- SDD11, SDD22 < -11dB for  $0.05 < f < f_b/7$  ( $f_b=28\text{GHz}$ )  
SDD11, SDD22 <  $-6.0 + 9.2 \cdot \log_{10}(2f/f_b)$  dB for  $f_b/7 < f < f_b$  ( $f_b=28\text{ GHz}$ )
- SDC11, SCD11 <  $-22 + 14 \cdot (f/f_b)$  dB for  $0.05 < f < f_b/2$  ( $f_b=28\text{ GHz}$ )  
SDC11, SCD11 <  $-18 + 6 \cdot f/f_b$  dB for  $f_b/2 < f < f_b$  ( $f_b=28\text{ GHz}$ )
- Ref OIF-CEI-28G-VSR as described in Implementation Agreement OIF-CEI-03.1
- SDD11, SDD22 < -11dB for  $0.05 < f < f_b/7$  ( $f_b=28\text{GHz}$ )  
SDD11, SDD22 <  $-6.0 + 9.2 \cdot \log_{10}(2f/f_b)$  dB for  $f_b/7 < f < f_b$  ( $f_b=28\text{ GHz}$ )
- SDC22, SCD22 <  $-25 + 20 \cdot (f/f_b)$  dB for  $0.05 < f < f_b/2$  ( $f_b=28\text{ GHz}$ )  
SDC22, SCD22 <  $-18 + 6 \cdot f/f_b$  dB for  $f_b/2 < f < f_b$  ( $f_b=28\text{ GHz}$ )
- Ref OIF-CEI-28G-VSR as described in Implementation Agreement OIF-CEI-03.1

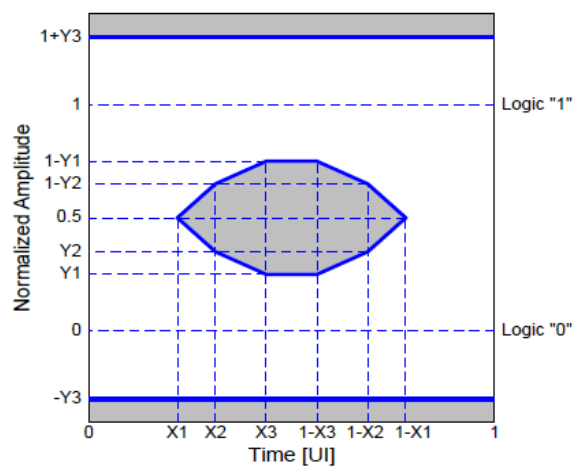
## Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
<b>Transmitter</b>						
Data Rate	fDC	25.78125			Gbps	1
Signal speed variation from nominal	$\Delta f_D$	-100		+100	ppm	
Transmitter center wavelength	$\lambda_C$	1320	1330	1340	nm	
Side Mode Suppression Ratio	SMSR	30			dB	
Average launch power	P <sub>Tavg</sub>	-5		+3	dBm	
Optical output power in OMA	OMA	-4		+2.2	dBm	
Launch power in OMA minus TDP		-5			dBm	
Transmitter and dispersion penalty (TDP)	TDP			2.7	dB	
Average launch power of OFF transmitter	P <sub>off</sub>			-30	dBm	
Extinction ratio	ER	3			dB	
Transmitter eye mask definition		Figure Below				
<b>Receiver</b>						
Receiver center wavelength	$\lambda_C$	1260	1270	1280	nm	
Receiver sensitivity in OMA	P <sub>minOMA</sub>			-12	dBm	2, 3
Stressed receiver sensitivity in OMA	P <sub>minSOMA</sub>			-9.5	dBm	2
Average received power	P <sub>Ravg</sub>			+2.2	dBm	

### Notes:

1. Testing by Data Rate; NRZ at 25.78125 Gbps, Mark Ratio 50%, PRBS=2<sup>31</sup>-1
2. For BER 5x10<sup>-5</sup>
3. Receiver Sensitivity in OMA is a normative specification.

### Mask of Optical Output Eye Diagram



X1	X2	X3	Y1	Y2	Y3	Max Hit Ratio (Note)
0.31	0.4	0.45	0.34	0.38	0.4	$5 \times 10^{-5}$

**Note:** The acceptable ratio of samples inside to outside the hatched area (the “hit ratio”) must be met.

#### Low Speed Control Pin Logic Levels

Parameter	Symbol	Min.	Max.	Unit	Conditions/Notes
Host VCC Range	Host_VCC	3.14	3.47	V	with $\pm 5\%$ variation
TX_Fault, RX_LOS	VOL	0.0	0.40	V	Note 1
	VIL	Host_VCC – 0.5	Host_VCC + 0.3	V	Note 1
TX_Disable	VIL	-0.3	0.8	V	Pulled up with 10k ohms to VccT in the module.
	VIH	2.0	VCC + 0.3	V	

#### Notes:

1. Rpullup (Rp) is the pull up resistor. Active bus termination may be used by the host in place of a pullup resistor. Pull ups can be connected to multiple power supplies, however the host board design shall ensure that no module pin has voltage exceeding module. Measured at the Host side of the connector.

**TX\_Fault** is a module output pin that when High, indicates that the module transmitter has detected a fault condition related to laser operation or safety. The TX\_Fault output pin is an open drain/collector and must be pulled up to the Host\_Vcc with 4.7k-10k $\Omega$  on the host board

**TX\_Disable** is a module input pin. When TX\_Disable is asserted High or left open, the SFP+ module transmitter output must be turned off. The TX\_Disable pin is pulled up to VccT with 10k $\Omega$  in the SFP+ module. The TX\_Disable pin works for TX\_fault\_Reset as well.

**Mod\_ABS** is pulled up to Host\_Vcc with 4.7k-10k $\Omega$  on the host board and connected to VeeT or VeeR in the SFP+ module. Mod\_ABS is then asserted “High” when the SFP+ module is physically absent from a host slot. In the SFP MSA (INF8074i) this pin had the same function but is called MOD\_DEF0.

**RX\_LOS** when high indicates an optical signal level below that specified in the relevant standard. The RX\_LOS pin is an open drain/collector output and must be pulled up to host Vcc with a 4.7k-10k $\Omega$  on the host board. RX\_LOS assert min and de-assert max are defined in the relevant standard.

### CDR Control for Bypass Mode

- Default value for “Soft RS0” and “Soft RS1” is ‘0’
- Hard pin#7 for RS0 and hard pin#9 for RS1 are terminated to Ground through 30kohm.

	Hard: Pin #7	Soft: A2h, Byte 110 bit 3	Mode of Operation
RS0	0	0	CDRR bypass mode
	0	1	CDRR engaged mode
	1	0	CDRR engaged mode
	1	1	CDRR engaged mode

	Hard: Pin #9	Soft: A2h, Byte 118 bit 3	Mode of Operation
RS1	0	0	CDRT bypass mode
	0	1	CDRT engaged mode
	1	0	CDRT engaged mode
	1	1	CDRT engaged mode

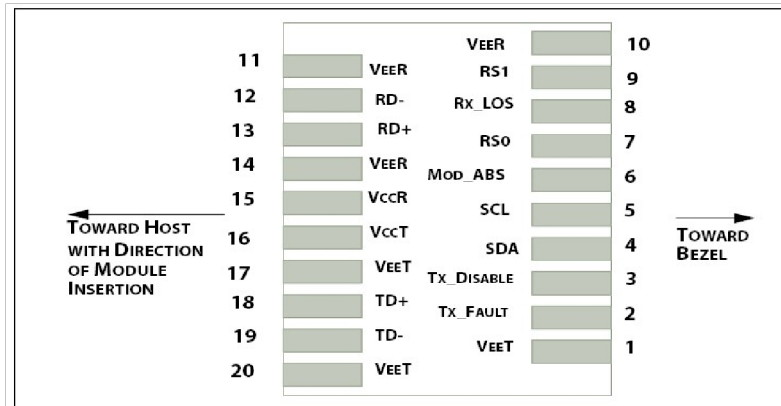
### Pin Description

PIN	Symbol	Name / Description	Notes
1	VeeT	Transmitter Ground	1
2	TX_Fault	Transmitter Fault (LVTTTL-O) - High indicates a fault condition	2
3	TX_Disable	Transmitter Disable (LVTTTL-I) – High or open disables the transmitter	3
4	SDA	Two wire serial interface Data Line (LVCMOS-I/O) (MOD-DEF2)	4
5	SCL	Two wire serial interface Clock Line (LVCMOS-I/O) (MOD-DEF1)	4
6	MOD_ABS	Module Absent (Output), connected to VeeT or VeeR in the module	5
7	RS0	NA	6
8	RX_LOS	Receiver Loss of Signal (LVTTTL-O)	2
9	RS1	NA	6
10	VeeR	Receiver Ground	1
11	VeeR	Receiver Ground	1
12	RD-	Inverse Received Data out (CML-O)	
13	RD+	Received Data out (CML-O)	
14	VeeR	Receiver Ground	1
15	VccR	Receiver Power - +3.3V	
16	VccT	Transmitter Power - +3.3 V	
17	VeeT	Transmitter Ground	1
18	TD+	Transmitter Data In (CML-I)	
19	TD-	Inverse Transmitter Data In (CML-I)	
20	VeeT	Transmitter Ground	1

**Notes:**

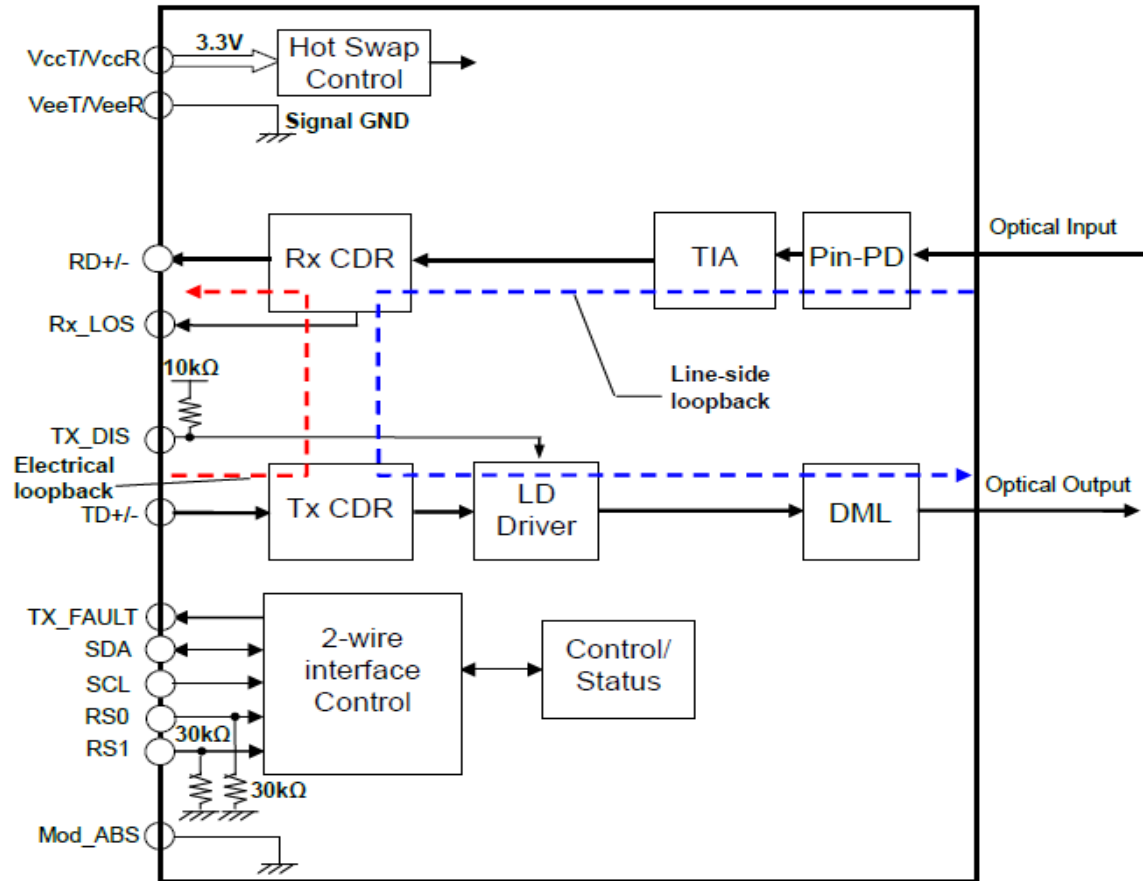
1. The module signal grounds are isolated from the module case.
2. This is an open collector/drain output that on the host board requires a 4.7KΩ to 10KΩ pull-up resistor to VccHost.
3. This input is internally biased high with a 4.7KΩ to 10KΩ pull-up resistor to VccT.
4. Two-Wire Serial interface clock and data lines require an external pull-up resistor dependent on the capacitance load.
5. This is a ground return that on the host board requires a 4.7KΩ to 10KΩ pull-up resistor to VccHost.
6. Rate select can also be set through the 2-wire bus in accordance with SFF-8472 v. 12.1, Rx Rate Select is set at Bit 3, Byte 110, Address A2h. Tx Rate Select is set at Bit 3, Byte 118, Address A2h.

Note: writing a “1” selects maximum bandwidth operation. Rate select is the logic OR of the input state of Rate Select Pin and 2-wire bus.



Pin-out of connector Block on Host board

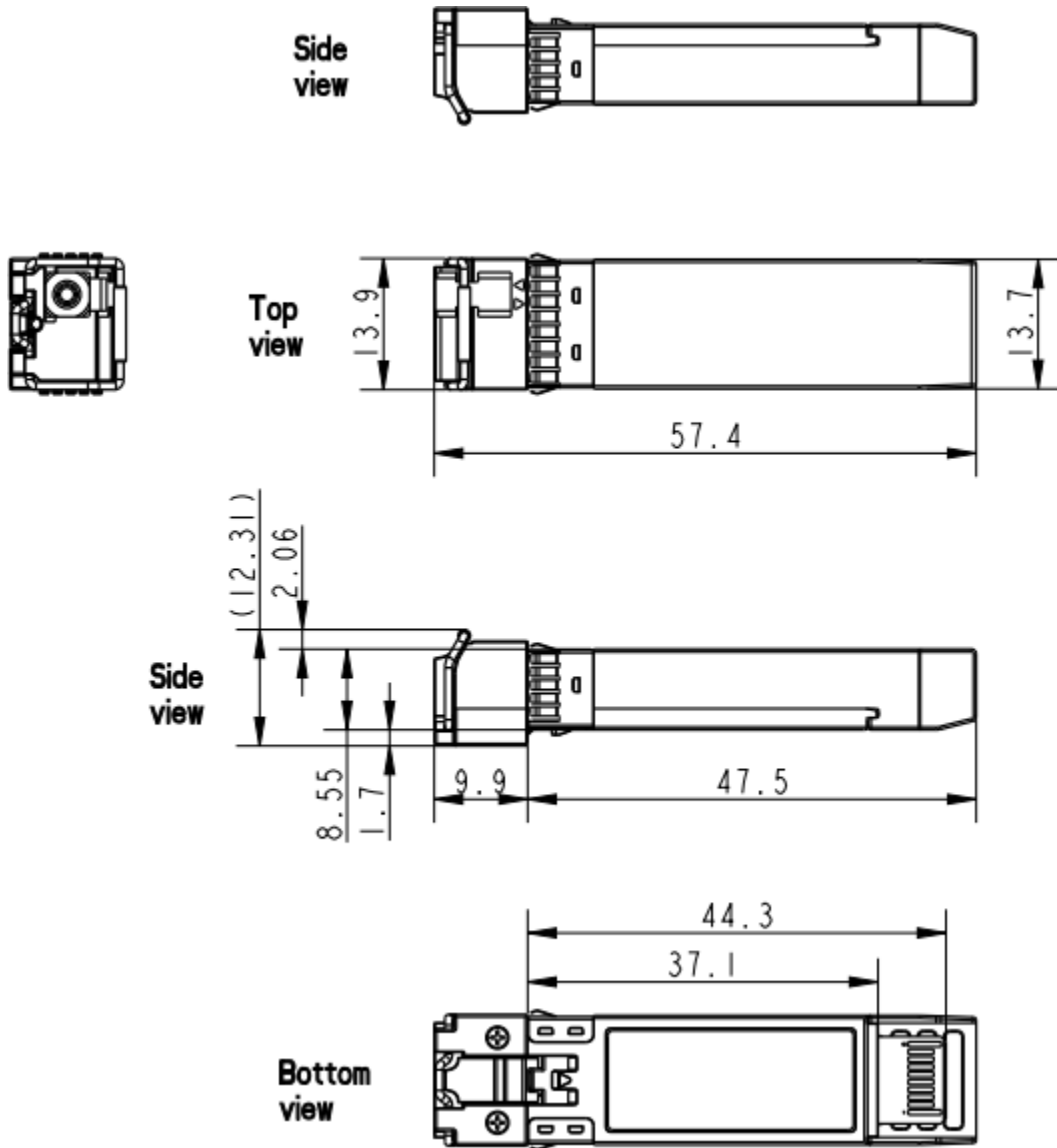
# Functional Block Diagram





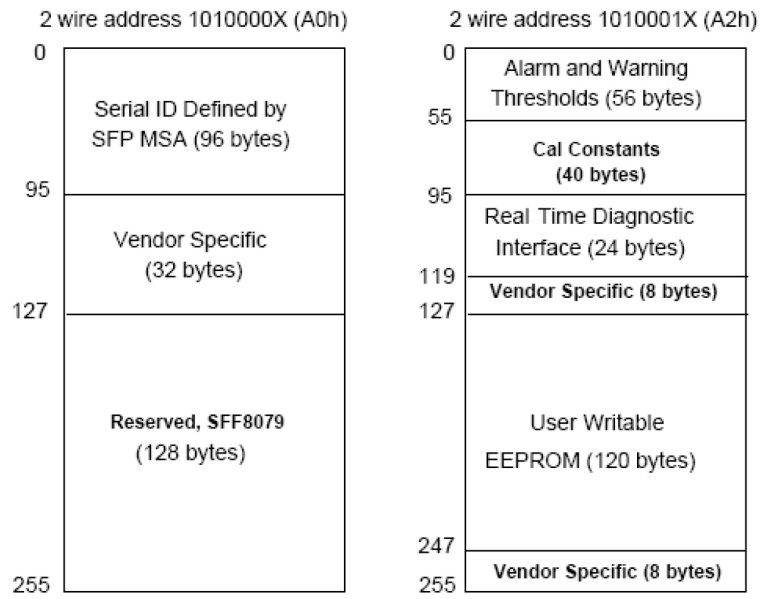
### Mechanical Specifications

Small Form Factor Pluggable (SFP) transceivers are compatible with the dimensions defined by the SFP Multi-Sourcing Agreement (MSA).



## EEPROM Information

EEPROM memory map specific data field description is as below:



## **About AddOn Networks**

In 1999, AddOn Networks entered the market with a single product. Our founders fulfilled a severe shortage for compatible, cost-effective optical transceivers that compete at the same performance levels as leading OEM manufacturers. Adhering to the idea of redefining service and product quality not previously had in the fiber optic networking industry, AddOn invested resources in solution design, production, fulfillment, and global support.

Combining one of the most extensive and stringent testing processes in the industry, an exceptional free tech support center, and a consistent roll-out of innovative technologies, AddOn has continually set industry standards of quality and reliability throughout its history.

Reliability is the cornerstone of any optical fiber network and is engrained in AddOn's DNA. It has played a key role in nurturing the long-term relationships developed over the years with customers. AddOn remains committed to exceeding industry standards with certifications from ranging from NEBS Level 3 to ISO 9001:2005 with every new development while maintaining the signature reliability of its products.

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